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INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT

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Complete If Known

Application Number	09/847,642
Filing Date	May 1, 2001
First Named Inventor	Mihai T. Lazarescu
Group Art Unit	2124
Examiner Name	INGBERG

Attorney Docket Number 261/246

## OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
TI	AA	Prof. Dov Dori, <u>About OPCAT</u> , 2000, pages 1-2, <a href="http://iew3.technion.ac.il/~dori/opcat/about.htm1">http://iew3.technion.ac.il/~dori/opcat/about.htm1</a>	
TS	AB	Prof. Dov Dori, <u>OPM Methodology</u> , 2000, pages 1-3, <a href="http://iew3.technion.ac.il/~dori/opcat/methodology.htm1">http://iew3.technion.ac.il/~dori/opcat/methodology.htm1</a>	
TF	AC	Prof. Dov Dori; <u>OPCAT's Contents</u> , 2000, pages 1-5, <a href="http://iew3.technion.ac.il/~dori/opcat/contents.htm1">http://iew3.technion.ac.il/~dori/opcat/contents.htm1</a>	
TX	AD	Prof. Dov Dori; <u>Examples</u> , 2000, pages 1-3 <a href="http://iew3.technion.ac.il/~dori/opcat/example.htm1">http://iew3.technion.ac.il/~dori/opcat/example.htm1</a> (Fig. 1 and Fig. 2 did not display when website was viewed).	
TX	AE	Vojin Zivojnovic, Stefan Pees, Christian Schlaeger, Markus Willems, Rainer Schoenen and Heinrich Meyr; <u>DSP Processor/Complier Co-Design A quantitative Approach</u> , ICSPAT, 1997, pages 761 - 765	
TX	AF	Guido Post, Vojin Zivojnovic and Sebastian Ritz; <u>Multiprocessor, Architecture Extension for the BlockDiagram-Oriented Design Tool Cossap/Descartes</u> , ICSPAT, 1995	
TX	AG	Stefan Pees, Vojin Zivojnovic, Andreas Hoffmann, Heinrich Meyr; <u>Retargetable Timed Instruction Set Simulation of Pipelined Processor Architectures</u> , ICSPAT, 1998	
TX	AH	Marcello Lajolo, Mihai Lazarescu, Alberto Sangiovanni-Vincentelli, <u>A Compilation-based Software Estimation Scheme for Hardware/Software Co-Simulation</u> , CODES, 1999	105 Regres
TX	AI	Mihai T. Lazarescu, Jwahar R. Bamm, Edwin Harcourt, Luciano Lavagno, Marcello Lajolo, <u>Compilation-based Software Performance Estimation for System Level Design</u> , HLDVT, November 8, 2000, pages 1-6	
TX	AJ	Graham R. Hellestrand, <u>Designing System on a Chip Products Using Systems Engineering Tools</u> , 1999, pages 1-6, VaST Systems Technology Corporation	
TX	AK	Vojin Zivojnovic, Stefan Pees, Heinrich Meyr, <u>LISA - Machine Description Language and Generic Machine Model for HW/SW Co-Design</u> , October 1996, 1996 IEEE Workshop on VLSI Signal Processing, San Francisco	
TX	AL	Vojin Zivojnovic, Steven Tjian, Heinrich Meyr, <u>Complied Simulation of Programmable DSP Architectures</u> , 1995, pp. 187-196, In the Proceedings of the 1995 IEEE Workshop on VLSI Signal Processing	
TX	AM	Vojin Zivojnovic, Juan Martinez Velarde, Christian Schlager, Heinrich Meyr, <u>Integrated Systems for Signal Processing</u> , E.E. Times, October 17, 1994, Issue: 819 pages 1-5, <a href="http://content.techweb.com/se/directlink.cgi?EET19941017S0055">http://content.techweb.com/se/directlink.cgi?EET19941017S0055</a>	
TX	AN	Vojin Zivojnovic, Stefan Pees, Christian Schlager, Heinrich Meyr, <u>Signal Processing Design, LISA bridges gaps in high-tech languages</u> , E.E. Times, October 7, 1996, Issue: 922, pages 1-6, <a href="http://content.techweb.com/se/directlink.cgi?EET19961007S0138">http://content.techweb.com/se/directlink.cgi?EET19961007S0138</a>	
TX	AO	V. Zivojnovic, S. Pees, <u>Complied DSPs check out fast</u> , E.E. Times, October 23, 1995, Issue: 871, Section: Digital Signal Processing, Pages 1-5, <a href="http://content.techweb.com/se/directlink.cgi?EET19951023S0056">http://content.techweb.com/se/directlink.cgi?EET19951023S0056</a>	
TX	AP	Vojin Zivojnovic, Heinrich Meyr, <u>Complied HW/SW Co-Simulation</u> , 1996, Integrated Systems for Signal Processing, Aachen University of Technology, Aachen, Germany	
TX	AQ	Dr. Graham Hellestrand, <u>The Advent of the Virtual Processor Model</u> , E. E. Times, May 14, 1999, pages 1-7, VaST Systems Technology, Santa Clara, CA, USA	
TX	AR	Graham R. Hellestrand, <u>Systems Engineering: The Era of the Virtual Processor Model (VPM)</u> , April 14, 1999, pages 1-6, VaST Systems Technology, Santa Clara, CA, USA	
TX	AS	Stephan Ohr, <u>Nonlinear Tips Analog Synthesis</u> , E. E. Times, June 12, 2001, Pages 1-3, Com, <a href="http://www.eetimes.com/story/OEG20010612S0067">http://www.eetimes.com/story/OEG20010612S0067</a>	

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First Named Inventor	Mihai T. Lazarescu
Group Art Unit	2124
Examiner Name	I WGBERG

TR	AT	Soner Önder, Rajiv Gupta, <u>Automatic Generation of Microarchitecture Simulators</u> , May 1998, IEEE International Conference on Computer Languages
TF	AU	Joachim Fitzner, ChrisSchläger, Davorin Mista, Vojin Zivojnovic, <u>Implementing LISA Tools Based on a DSP Architecture Description</u> , ICSPAT 1999
TV	AV	Lisa Guerra, Joachim Fitzner, Dipankar Talukdar, Chris Schlager, Bassam Tabbara, Vojin Zivojnovic, <u>Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification</u> DAC 1999
TC	AW	Stafan Pees, Andreas Hoffmann, Vojin Zivojnovic, Heinrich Meyr, <u>LISA - Machine Description Language for Cycle-Accurate Models of Programmable DSP Architectures</u> , DAC 1999
TX	AX	Chris Schlager, Joachim Fitzner, Vojin Zivojnovic, <u>Using Supersim Complied Processor Models for Hardware, Software and System Design</u> , ICSPAT 1998
TX	AY	Vojin Zivojnovic, Chris Schlager, Joachim Fitzner, <u>System-Level Modeling of DSP and Embedded Processors</u> , ASIOMAR 1998

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